REMARKS

The following remarks are made in response to the Non-Final Office Action mailed August 20, 2010. Claims 20-39 were rejected. With this Response, no claims have been amended. Claims 20-39 remain pending in the application and are presented for reconsideration and allowance.

In the Title

The Examiner objected to the title of the invention because the title is not descriptive enough. Applicant has amended the title to correct this informality. Applicant believes the title is now in condition for allowance.

Claim Rejections under 35 U.S.C. § 103

The Examiner rejected claims 20-39 under 35 U.S.C. § 103(a) as being unpatentable over the Gorbet et al. U.S. Patent No. 5,941,714 in view of the D'Angelo U.S. Patent Application Publication No. 2002/0030475 and the Duley U.S. Patent No. 6,766,222. Applicant respectfully disagrees.

Claim 20 is a processor array including a multiplicity of processor elements. Each processor element includes at least one processor and a plurality of power supply interfaces for transmitting electricity from and to a plurality of processor elements adjacent to the respective processor element. Each also includes a plurality of ***power supply switches, each power supply interface being assigned a power supply switch***, with which electricity can be supplied or not supplied to the respective power supply interface as desired. Each include ***testing means for sequentially testing*** whether there is an electrical short-circuit at a power supply interface to a couple adjacent processor element. Each also include control means for closing the respective power supply switch so that electricity can be supplied to the power supply interface when there is no short-circuit on the power supply interface. At least to some extent, only the processor elements that are arranged locally directly adjacent to one another are coupled to one another in order to exchange electronic messages and to transmit electricity. This is not taught or suggested.

The control means, recited in claim 20, closes off the power supply interfaces in a controlled manner, without the risk that an electric short-circuit between two processor elements destroys the whole processor assembly. Each processor element of the processor array includes a plurality of power supply switches, wherein by using an energy supply of an energy supply interface assigned to the switch electrical energy is supplied or is not supplied depending on the result of a short-circuit testing. The short-circuit testing is carried out using a short-circuit test unit formed in the processor element, which short-circuit testing unit sequentially tests if an electrical short-circuit with a connected adjacent processor element occurs at one of the respective energy-supply-interfaces of the processor element. The selective supply of electrical energy to an energy supply interface is carried out using a control unit formed in the processor element, which control unit is set up such that, in case there is no short-circuit on the energy supply interface, the respective energy supply switch is closed such that electric current can be supplied to the energy supply interface. Accordingly, the processor array of claim 20 prevents the breakdown of the entire processor array, even in case of an occurring short-circuit in a processor array having a plurality of processor elements connected to each other. This is not taught or suggested in the art of record.

The Gorbet et al. patent describes a processor assembly having a plurality of processor elements coupled to one another, wherein each processor element comprises an energy regulation circuit (col. 5, line 18), through which the energy supply and communications signals pass. In order to ensure a faultless signal and energy transmission even through contacts connected to one another, the mechanical contact of which is not ideal, a higher voltage (for example 12V) is applied to the power contacts, which is higher than the voltage, which is necessary for operating the processor circuit (for example standard 5V TTL level). The energy regulation circuit of the processor element serves in this context to convert down the higher voltage applied to the voltage supply contacts to the lower level necessary for operating the processor circuit. Furthermore, in the Gorbet et al. patent, a voltage can be supplied to a processor assembly through a plurality of interfaces of a plurality of adjacent processor elements. In this context, the energy regulation circuit of a processor element is used to ensure independent from the number of active voltage connections to adjacent processor elements in each case a constant input voltage for the circuit of the processor element. For achieving

of the above-mentioned functions, the disclosed energy regulation circuit comprises a voltage regulator.

The Gorbet et al. Patent, however, does not describe ***energy supply switches*** that are ***each assigned to an energy supply interface*** by use of which depending on a short-circuit test energy is suppliable to the respective energy supply interface or not. Furthermore, the Gorbet et al. patent does not describe a ***short-circuit testing unit*** and no control unit for closing a respective energy supply switch, in case there is no short-circuit. Furthermore, the Gorbet et al. patent does not give any hint for ***sequentially testing*** using the short-circuit testing unit, if an electrical short circuit at an energy supply interface with a connected adjacent processor element occurs at an energy supply. The energy regulation circuit described in the Gorbet et al. patent does not serve to sequentially test, if an electrical short circuit at an energy supply interface with a connected adjacent processor element occurs at an energy supply nor, in case there is no short-circuit at the energy supply interface, to close a respective energy supply switch such that electric energy can be supplied to the energy supply interface.

Quite the contrary, the energy regulation circuit described in the Gorbet et al. patent converts down a higher voltage applied to the power contacts to a lower level appropriate for the processor circuit. Hence, an assembly, which is used for protecting a processor element of the processor array from a short-circuit, by testing, before supplying electrical energy to an energy supply interface, if there is a short-circuit at this energy supply interface, is not disclosed in the Gorbet et al. patent nor does the Gorbet et al. patent give any hint fort this advantageous solution. In fact, the Gorbet et al. patent even does not give any hint for the arise of the problem of an electrical short-circuit.

The D'Angelo publication does not give any hint for the processor array according to claim 20. In fact, the D'Angelo publication merely describes the use of a power MOSFET switch for limiting the current passing through the switch when a load becomes short-circuited. Hence, the D'Angelo publication does not give any hint for integrating a short-circuit protection assembly in the specific assembly of a processor array according to claim 20.

In col. 3, line 6 of the Duley patent, a test rack is mentioned, which is merely used for monitoring the reduction of the inrush current to 1/16 of the value what it would be if all the loads

were energized at once. The Duley patent describes the sequential and delayed switch-on of different loads for minimizing the possibility of component stress.

However, the Duley patent does not describe the testing unit according to claim 20 nor the application of a control of the current in a network, wherein each processor element can have adjacent processor elements and current can be supplied from adjacent processor elements to each other. As is evident from a review of Figure 1 in the Duley patent, merely a star-shaped current supply is illustrated. Hence, the Duley patent of course does not give any hint for the problem underlying claim 20 nor for the claimed solution. Therefore the Duley patent teaches away from subject matter of presently pending claim 20.

Consequently subject matter of presently pending claim 20 is novel and non-obvious in the light of cited prior art. For analogue reasons, independent claims 28, 37 and 38 are also novel and non-obvious over cited prior art, as are dependent claims 20-27, 29-36 and 39.

In view of the foregoing, reconsideration and allowance of currently pending claims 20 to 39 are solicited. Therefore, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection to the claims, and requests allowance of these claims.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 20-39 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 20-39 are respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

Please consider this a Petition for Extension of Time for a sufficient number of months to enter these papers, if appropriate. At any time during the pendency of this application, please charge any additional fees or credit overpayment to Deposit Account No. 500471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Paul P. Kempf at Telephone No. (612) 767-2502, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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